

CLAIMS

What is claimed is:

- 1 1. An apparatus for decoding and deinterleaving a received signal, the received signal
2 encoded with two constituent codes and interleaved on a frame by frame basis, the
3 apparatus comprising:
4 a single constituent code decoder; and
5 a single common buffer coupled to the single constituent code decoder, the common
6 buffer sized to hold a single frame of received data.
- 1 2. The apparatus of claim 1, further comprising:
2 an address controller coupled to the single common buffer, the address controller
3 generating read and write addresses that cause data to be de-interleaved when read
4 from and written to the common buffer and generating read and write addresses that
5 cause data to be interleaved when read from and written to the common buffer.
- 1 3. The apparatus of claim 2, wherein the address controller generates read and write
2 addresses that cause data to be read from the common buffer row by row and to be written
3 to the common buffer column by column to de-interleave the data and generates read and
4 write addresses that cause data to be read from the common buffer column by column and
5 to be written to the common buffer row by row to interleave the data.
- 1 4. The apparatus of claim 3, wherein the common buffer is divided into a plurality of sub-
2 buffers and each sub-buffer is a single port memory.
- 1 5. The apparatus of claim 4, wherein the address controller is configured to generate a read
2 address for one of the plurality of sub-buffers and a write address for another of the
3 plurality of sub-buffers, the reading and writing of the respective sub-buffers to occur
4 during the same clock cycle.

- 1 6. The apparatus of claim 2, wherein the address controller employs a first algorithm to
2 generate read addresses for the common buffer for data input to the constituent code
3 decoder and contemporaneously employs the first algorithm to generate write addresses
4 for the common buffer for data output from the constituent code decoder where the write
5 addresses are offset by a predetermined number of rows from the read addresses when the
6 decoder is decoding the first of the two constituent codes.

- 1 7. The apparatus of claim 6, wherein the address controller employs a second algorithm to
2 generate read addresses for the common buffer for data input to the constituent code
3 decoder and contemporaneously employs the second algorithm to generate write addresses
4 for the common buffer for data output from the constituent code decoder where the write
5 addresses are offset by a predetermined number of columns from the read addresses when
6 the decoder is decoding the second of the two constituent codes.

- 1 8. The apparatus of claim 7, wherein the employment of the first algorithm to generate write
2 addresses during the decoding of the first of the two constituent codes and employment of
3 the second algorithm to generate read addresses during the decoding of the second of the
4 two constituent codes interleaves the data and the employment of the second algorithm to
5 generate write addresses during the decoding of the second of the two constituent codes
6 and employment of the first algorithm to generate read addresses during the decoding of
7 the first of the two constituent codes de-interleaves the data.

- 1 9. The apparatus of claim 8, wherein the address controller is configured to generate read
2 addresses using a one of a row-by-row with column shuffling algorithm and a column-by-
3 column with row shuffling algorithm.

- 1 10. The apparatus of claim 9, wherein the received signal is encoded with two constituent
2 codes and interleaved based on a CDMA protocol and wherein the apparatus is employed
3 in a mobile unit deployed within a CDMA-based communication system.
- 1 11. A method of decoding and deinterleaving a received signal, the received signal encoded
2 with two constituent codes and interleaved on a frame by frame basis, the method
3 comprising the steps of:
4 serially decoding the received signal; and
5 storing received data and decoded data in a single common buffer, the common buffer
6 sized to hold a single frame of received data.
- 1 12. The method of claim 11, further comprising the step of:
2 a) generating read and write addresses that cause data to be de-interleaved when
3 read from and written to the common buffer and generating read and write addresses
4 that cause data to be interleaved when read from and written to the common buffer.
- 1 13. The method of claim 12, wherein step a) generates read and write addresses that cause
2 data to be read from the common buffer row by row and to be written to the common
3 buffer column by column to de-interleave the data and generates read and write addresses
4 that cause data to be read from the common buffer column by column and to be written to
5 the common buffer row by row to interleave the data.
- 1 14. The method of claim 13, wherein the common buffer is divided into a plurality of sub-
2 buffers and each sub-buffer is a single port memory.

- 1 15. The method of claim 14, further comprising the step of generating a read address for one
2 of the plurality of sub-buffers and a write address for another of the plurality of sub-
3 buffers, the reading and writing of the respective sub-buffers occurring during the same
4 clock cycle.
- 1 16. The method of claim 12, wherein step a) includes the step of employing a first algorithm
2 to generate read addresses for the common buffer for data input to the constituent code
3 decoder and contemporaneously employing the first algorithm to generate write addresses
4 for the common buffer for data output from the constituent code decoder where the write
5 addresses are offset by a predetermined number of rows from the read addresses when the
6 decoder is decoding the first of the two constituent codes.
- 1 17. The method of claim 16, wherein step a) includes the step of employing a second
2 algorithm to generate read addresses for the common buffer for data input to the
3 constituent code decoder and contemporaneously employing the second algorithm to
4 generate write addresses for the common buffer for data output from the constituent code
5 decoder where the write addresses are offset by a predetermined number of columns from
6 the read addresses when the decoder is decoding the second of the two constituent codes.
- 1 18. The method of claim 17, wherein the employment of the first algorithm to generate write
2 addresses during the decoding of the first of the two constituent codes and employment of
3 the second algorithm to generate read addresses during the decoding of the second of the
4 two constituent codes interleaves the data and the employment of the second algorithm to
5 generate write addresses during the decoding of the second of the two constituent codes
6 and employment of the first algorithm to generate read addresses during the decoding of
7 the first of the two constituent codes de-interleaves the data.

- 1 19. The method of claim 18, wherein step a) includes the step of generating read addresses
2 using a one of a row-by-row with column shuffling algorithm and a column-by-column
3 with row shuffling algorithm.
- 1 20. The method of claim 19, wherein the received signal is encoded with two constituent
2 codes and interleaved based on a CDMA protocol and wherein the apparatus is employed
3 in a mobile unit deployed within a CDMA-based communication system.
- 1 21. An article of manufacture for use in decoding and deinterleaving a received signal, the
2 received signal encoded with two constituent codes and interleaved on a frame by frame
3 basis, the article of manufacture comprising computer readable storage media including
4 program logic embedded therein that causes control circuitry to perform the steps of:
5 serially decoding the received signal; and
6 storing received data and decoded data in a single common buffer, the common buffer
7 sized to hold a single frame of received data.
- 1 22. The article of manufacture of claim 21, further performing the step of:
2 a) generating read and write addresses that cause data to be de-interleaved when
3 read from and written to the common buffer and generating read and write addresses
4 that cause data to be interleaved when read from and written to the common buffer.
- 1 23. The article of manufacture of claim 22, wherein step a) generates read and write addresses
2 that cause data to be read from the common buffer row by row and to be written to the
3 common buffer column by column to de-interleave the data and generates read and write
4 addresses that cause data to be read from the common buffer column by column and to be
5 written to the common buffer row by row to interleave the data.

- 1 24. The article of manufacture of claim 23, wherein the common buffer is divided into a
2 plurality of sub-buffers and each sub-buffer is a single port memory.
- 1 25. The article of manufacture of claim 24, the further performing the step of generating a
2 read address for one of the plurality of sub-buffers and a write address for another of the
3 plurality of sub-buffers, the reading and writing of the respective sub-buffers occurring
4 during the same clock cycle.
- 1 26. The article of manufacture of claim 22, wherein step a) includes the step of employing a
2 first algorithm to generate read addresses for the common buffer for data input to the
3 constituent code decoder and contemporaneously employing the first algorithm to
4 generate write addresses for the common buffer for data output from the constituent code
5 decoder where the write addresses are offset by a predetermined number of rows from the
6 read addresses when the decoder is decoding the first of the two constituent codes.
- 1 27. The article of manufacture of claim 26, wherein step a) includes the step of employing a
2 second algorithm to generate read addresses for the common buffer for data input to the
3 constituent code decoder and contemporaneously employing the second algorithm to
4 generate write addresses for the common buffer for data output from the constituent code
5 decoder where the write addresses are offset by a predetermined number of columns from
6 the read addresses when the decoder is decoding the second of the two constituent codes.

- 1 28. The article of manufacture of claim 27, wherein the employment of the first algorithm to
2 generate write addresses during the decoding of the first of the two constituent codes and
3 employment of the second algorithm to generate read addresses during the decoding of the
4 second of the two constituent codes interleaves the data and the employment of the second
5 algorithm to generate write addresses during the decoding of the second of the two
6 constituent codes and employment of the first algorithm to generate read addresses during
7 the decoding of the first of the two constituent codes de-interleaves the data.
- 1 29. The article of manufacture of claim 28, wherein step a) includes the step of generating
2 read addresses using a one of a row-by-row with column shuffling algorithm and a
3 column-by-column with row shuffling algorithm.
- 1 30. The article of manufacture of claim 29, wherein the received signal is encoded with two
2 constituent codes and interleaved based on a CDMA protocol and wherein the apparatus is
3 employed in a mobile unit deployed within a CDMA-based communication system.